Next-Generation Network SRAM

Agenda

- QDR™ Accomplishments
- QDRII/DDRII Specification Release
- Networking SRAM Evolution
- QDR Co-Development Strategy
- QDR Definition
- QDRI/QDRII Features and Benefits
- DDR Definition
- DDRI/DDRII Features and Benefits
- Timing Diagrams
- QDR Member Road Map

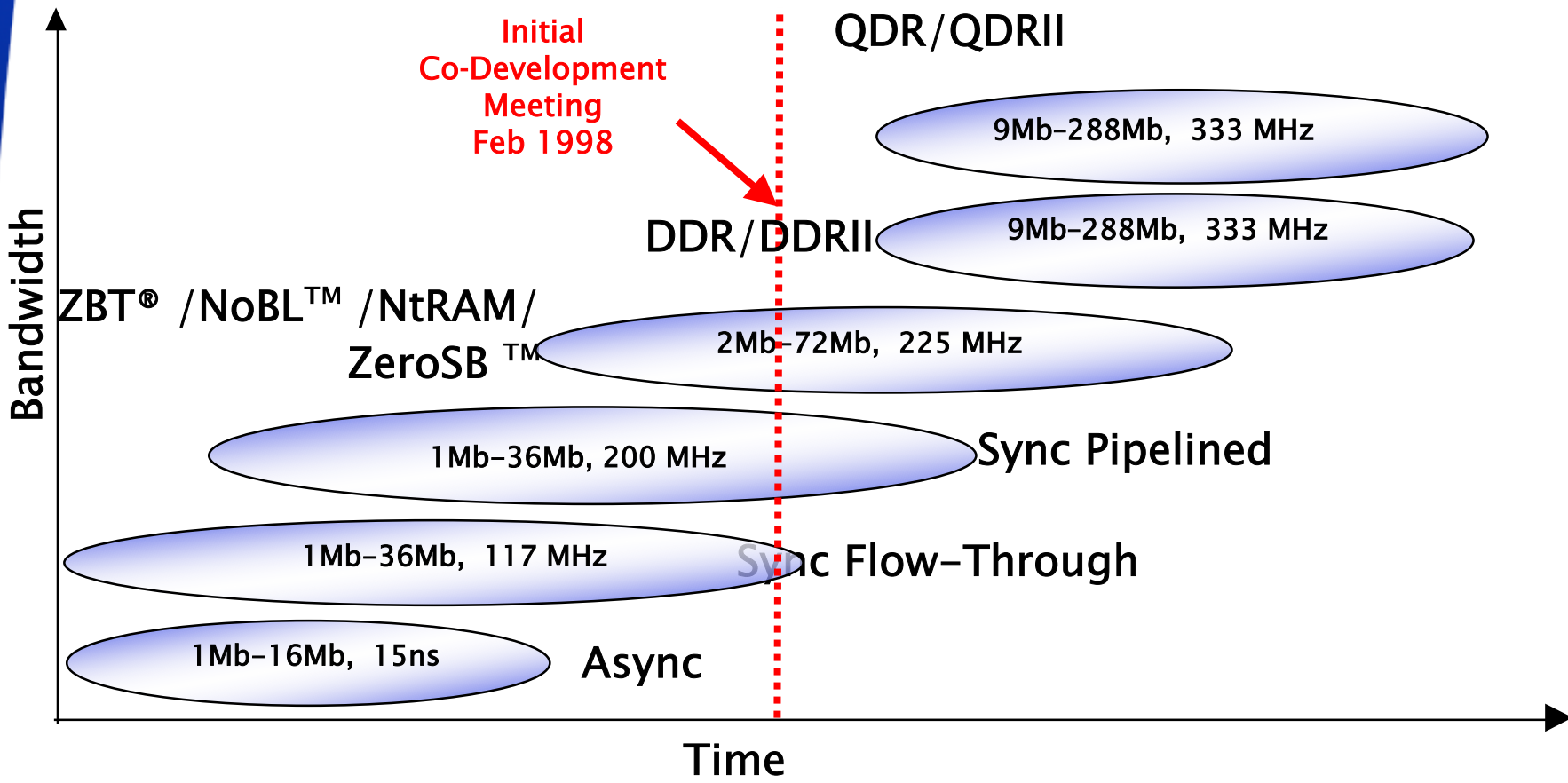
QDR Co-Development Accomplishments

- QDR Consortium Formed – Feb ’99
- QDRI Specifications Released – 2H99
- QDRII Defined – 2H00
- QDRI 9Mb Sampled – 1H01
- NEC Joins QDR Consortium – 1Q01
- Samsung Joins QDR Consortium – 2Q01
- Hitachi Signs LOI to Join QDR Consortium – 3Q01
- QDRII Specifications Released – 4Q01
- QDRII 18Mb Sampled – 4Q01

QDRII/DDRII Spec Release

- QDRII provides the necessary bandwidth in OC-768 applications: 36 Gb/s
- QDRII/DDRII complements a portfolio of products that can provide complete memory solutions for any networking system
- QDRII is supported by six SRAM vendors who provides 70% of the synchronous SRAM volume worldwide

Networking SRAM Evolution



ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc., and Motorola Inc. NoBL is a trademark of Cypress Semiconductor. NtRAM is a trademark of Samsung Semiconductor. ZeroSB is a trademark of NEC. QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress Semiconductor, IDT, NEC, Micron Technology, Inc., Samsung & Hitachi.

QDR Co-Development Strategy

- Provide high-performance, leading-edge, cost-effective, networking-optimized SRAMs
  - True, viable, reliable, multiple sources with standardized packaging, timing, functionality, etc.
  - Density and performance road map
  - Complete SRAM family portfolio for all networking systems: QDR and DDR
  - Time to market
  - In-house manufacturing capability

New SRAM Architectures

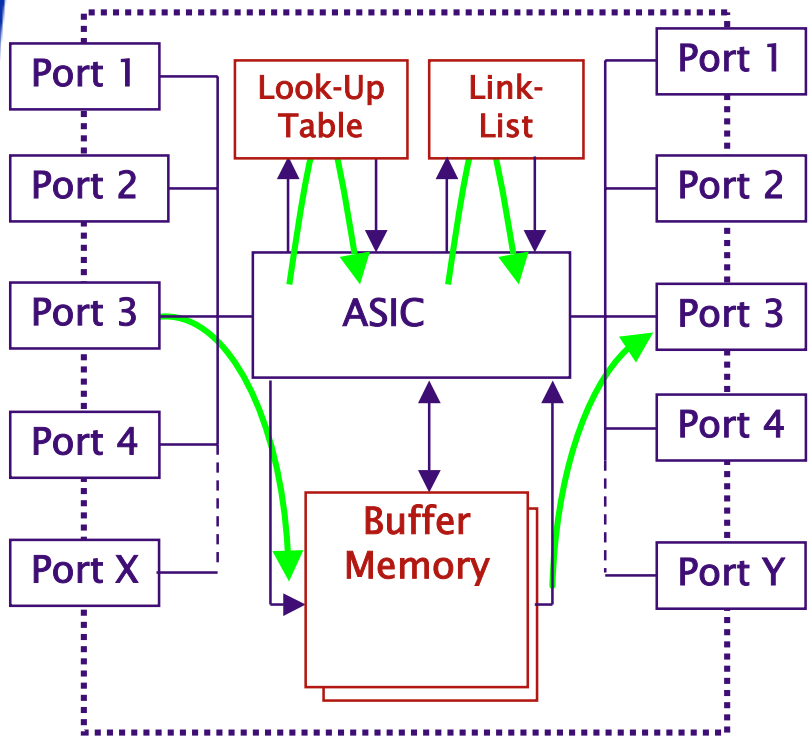
- **QDR** (2- or 4-word burst)
  - Separate D(in) and Q(out) buses
  - Separate/concurrent Read and Write ports
- **DDR Common I/O** (2- or 4-word burst)
  - Common DQ bus, common R/W bus
- **DDR Separate I/O** (2-word burst)
  - Separate D(in) and Q(out) buses
  - Separate/non-concurrent Read and Write ports
- All use HSTL I/O (1.5V or 1.8V)
  - Simulated to 1.8 GHz at 1.5V VDDQ

What is QDR?

Quad Data Rate SRAM – 2 READs and 2 WRITEs per clock

Design Issue	Feature	Benefit
Bandwidth	Separate I/Os	No contention, high frequency
	Innovative architecture	High bus utilization
	DDR interfaces	Higher Mb/s
	HSTL I/O levels	Higher frequency potential
Initial Latency	2-stage pipeline	Low initial latency
Density	9Mb now, 18Mb 4Q01	Compatible migration
Cost/Availability	State-of-the-art process	Low cost structure
Alternate Sources	Cypress, Hitachi, IDT, Micron, NEC, and Samsung	Security of supply

QDR Network Solutions

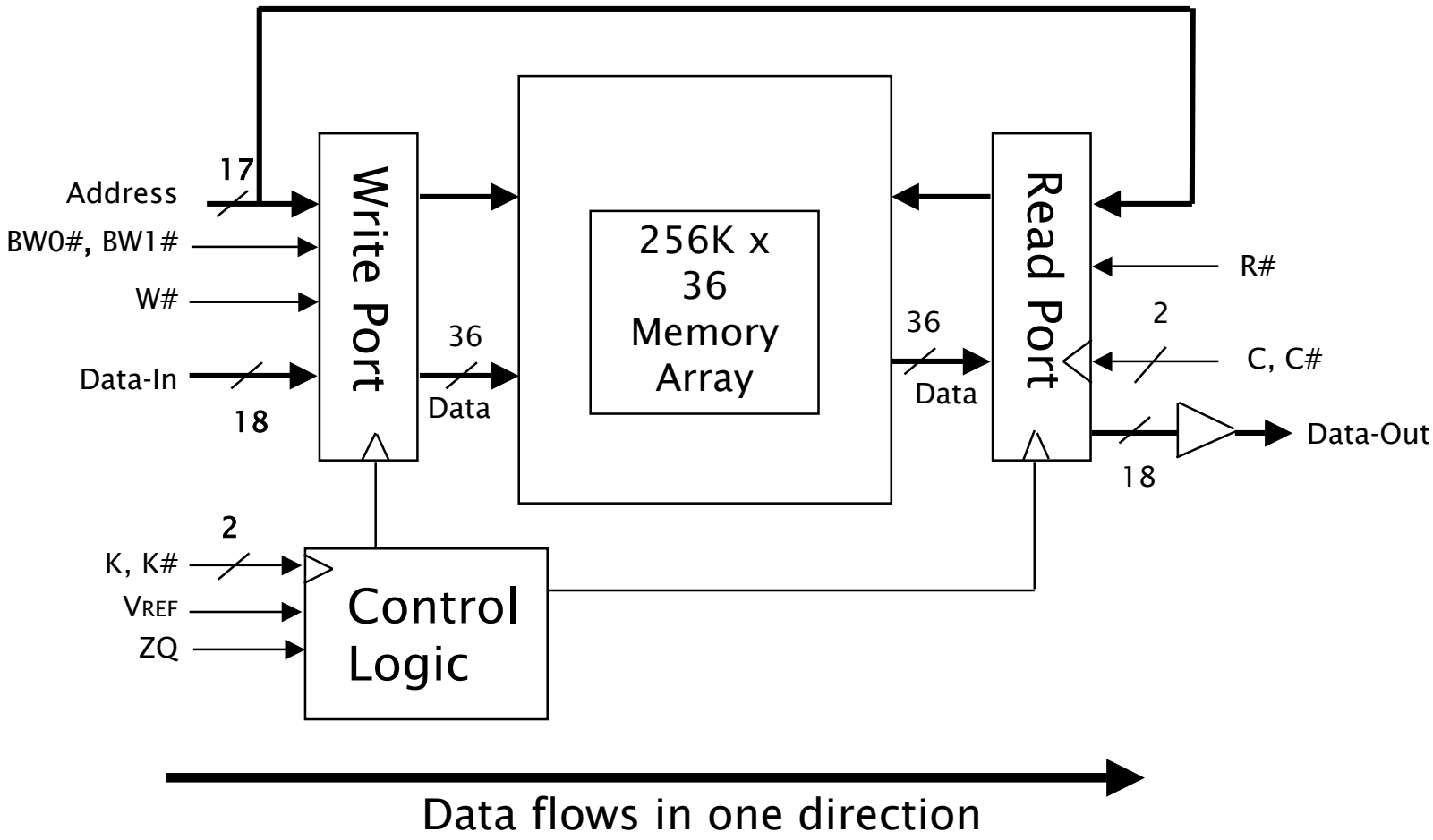


Data flows in one direction

Customer Design Issues:

1. Bandwidth	666 MHz+/pin
2. Initial Latency	6ns
3. Density	9Mb, 18Mb+
4. Cost	Competitive
5. Sourcing	Cypress,Hitachi IDT, Micron, NEC, and Samsung

Block Diagram



QDR Features and Benefits

Features	Benefits
* Simultaneous Accesses	* Simpler Memory Utilization and Improved Bandwidth (~2x)
* DDR Interface on Both Ports	* Improved Bandwidth (~2x)
* 2-Stage Pipeline	* Low Initial Latency
* Separate Input/Output Ports	* No Bus Contention
* 165-ball FBGA Package	* Small Board Area (40%<BGA)
* Separate Clocks for I/P and O/P	* Can Skew Input and Output
* Wide Voltage Range (HSTL I/O)	* Simplified Selection of System Voltage Supply
* Programmable I/O Impedance Lines	* Reduced Noise on Output

QDRII Features and Benefits

Features	Benefits
* 250 MHz Operation	* 36 Gb/s R/W on a x36 QDR
* 333 MHz Operation	* 48 Gb/s R/W on a x36 QDR
* DLL	* Increased Data Valid Time (up to 65% of Cycle)
* 2.5-Stage Pipeline	* Low Initial Latency
* Echo Clocks	* Simplifies Data Capture
	* Guaranteed Relationship to Valid Data (200ps prior)
* 165-ball FBGA Package	* Compatible with Standard QDR Pinout

QDR VS. QDRII
Feature Comparison

	QDRI	QDRII
Frequency		
2-Word burst	166 MHz	250 MHz
4-Word burst	200 MHz	333 MHz
Data Valid Window	1.4ns @166 MHz	1.9ns @166 MHz 0.98ns @333 MHz
Latency	2 Cycles	2.5 Cycles
Clocks	No Echo CLKs	Echo CLKs
Density	9/18/36Mb	18/36/72Mb+
VCC	2.5V	1.8V

What is DDR?

Double Data Rate SRAM – 2 READs or 2 WRITEs per clock

Design Issue	Feature	Benefit
Bandwidth	DDR interfaces	Higher Mb/s
	HSTL I/O levels	Higher frequency potential
Initial Latency	2-stage pipeline	Low initial latency
Density	18Mb 1Q02	
	36Mb 3Q02	Compatible migration
Cost/Availability	State-of-the-art process	Low cost structure

Alternate Sources: Cypress, Hitachi, IDT, Micron, Security of supply NEC, and Samsung

DDR Features and Benefits

Features

* DDR interface on both ports
* 2-Stage pipeline
* HSTL I/Os
* Separate echo clocks
* 165-ball FBGA package

Benefits

* Improved bandwidth(~2x)
* Low initial latency
* Allows frequency migration
* Simplifies data capture
* Small board area

DDRII Features and Benefits

Features

* 333 MHz operation
* 2.5-Stage pipeline
* 165-ball BGA package

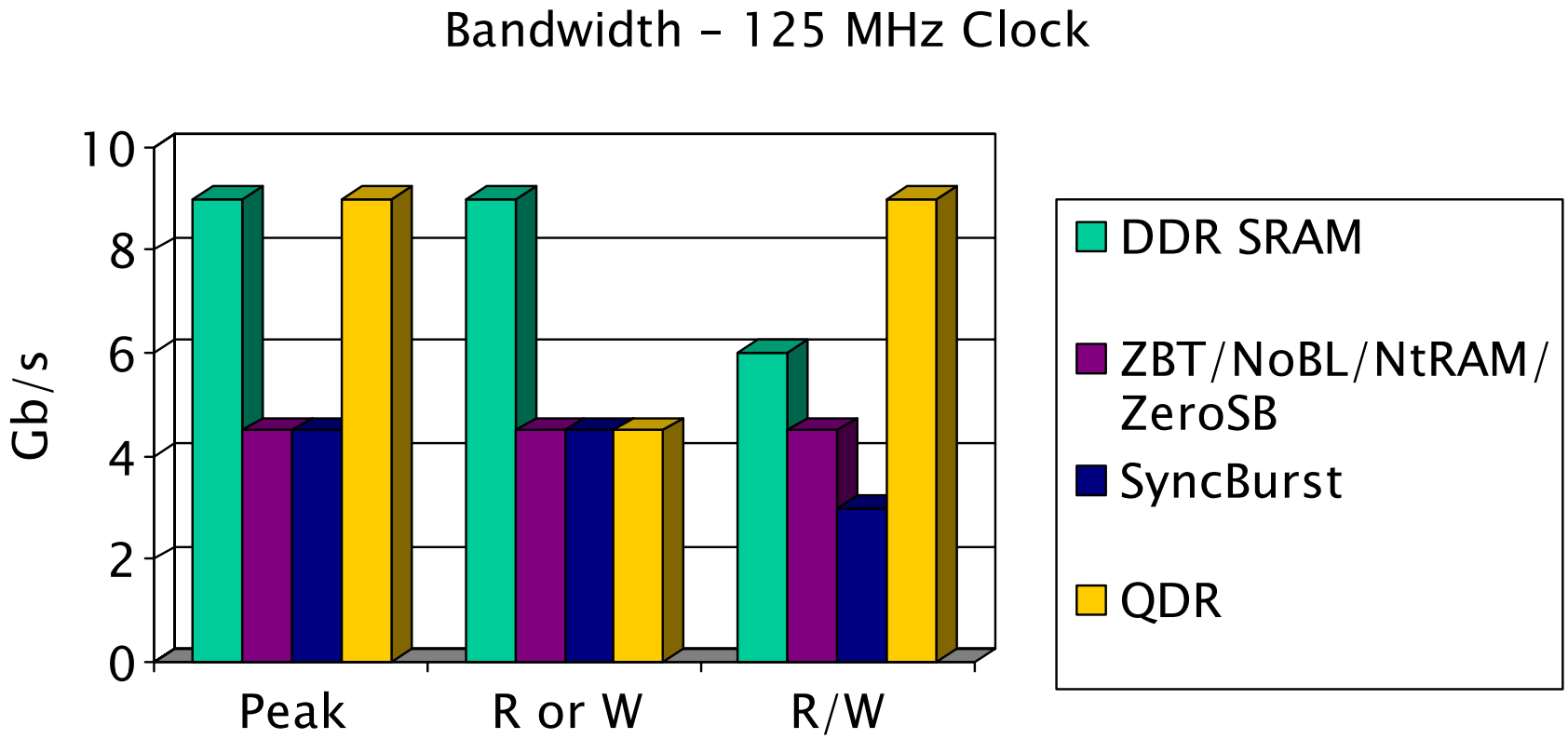
Benefits

* Higher bandwidth
* Low initial latency
* Small board area

DDR vs. DDRII Feature Comparison

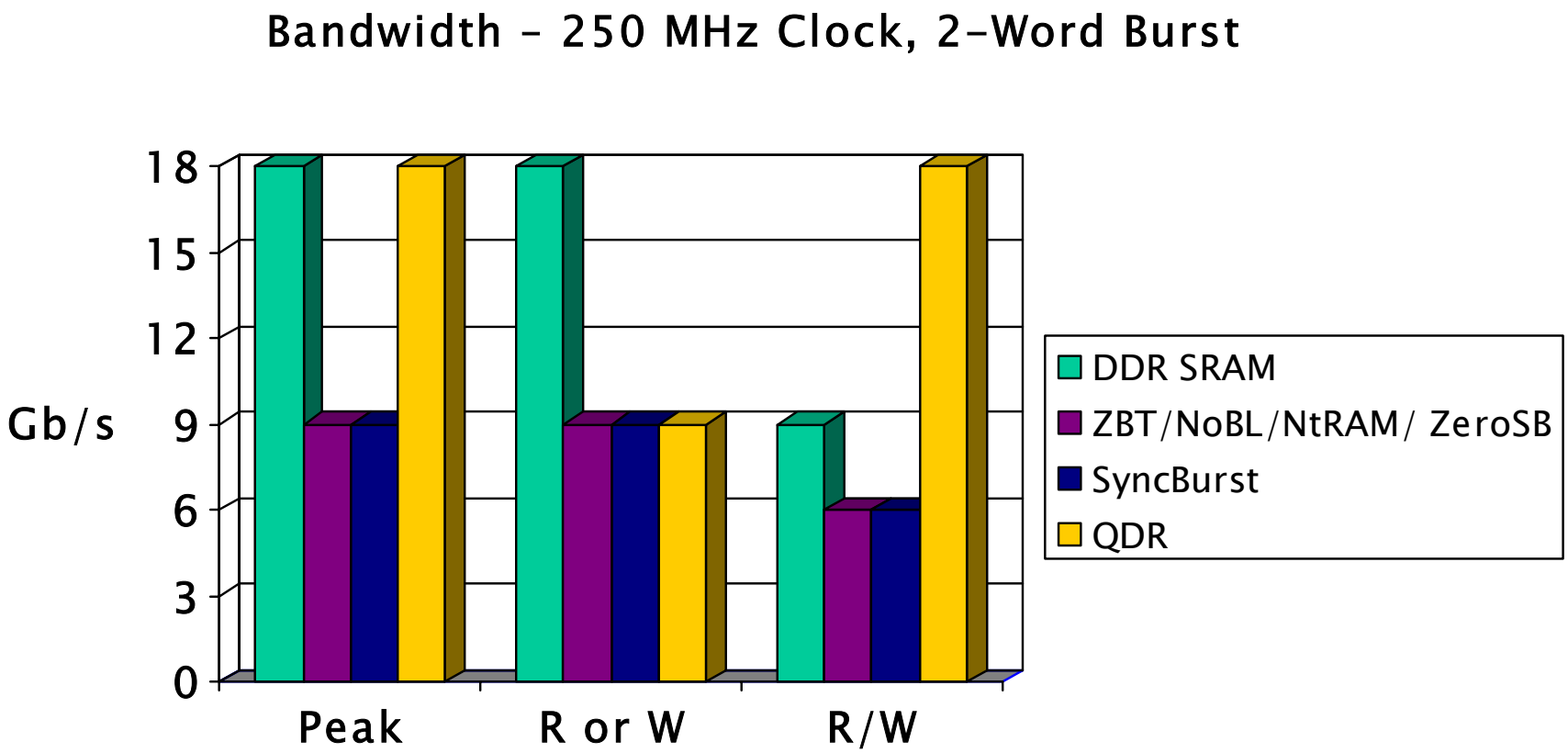
	DDRI	DDRII
Frequency		
2-Word Burst	N/A	333 MHz
4-Word Burst	200 MHz	333 MHz
Data Valid Window	1.4ns @166 MHz	1.9ns @ 166 MHz 0.98ns @ 333 MHz
Latency	2 cycles	2.5 cycles
Density	9/18/36Mb	18/36/72Mb+
VCC	2.5V	1.8V

Architectural Comparison



Note: Assumes single x18 (per port) QDR device versus x36 width on the other devices.

Bandwidth Comparison



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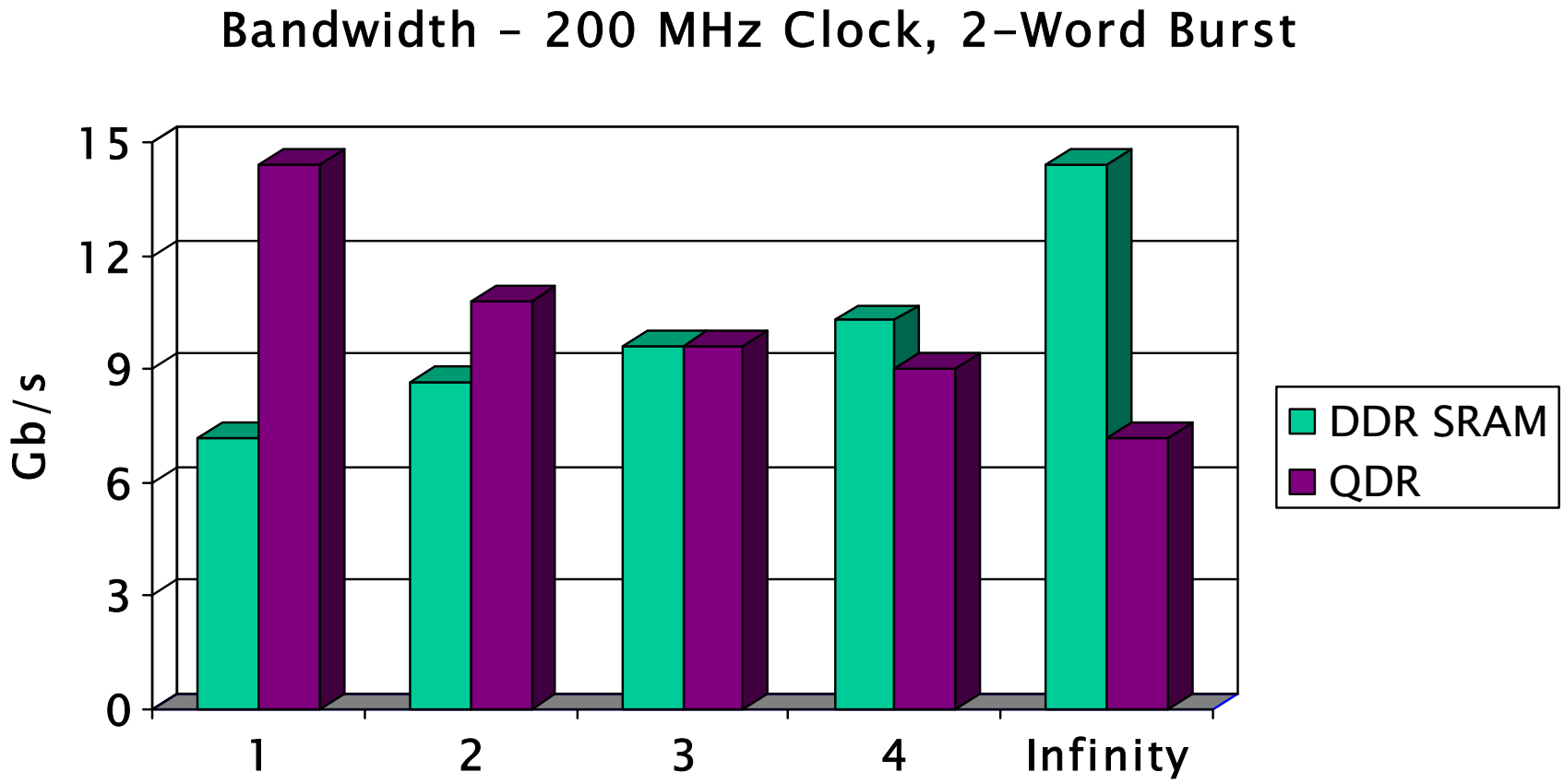
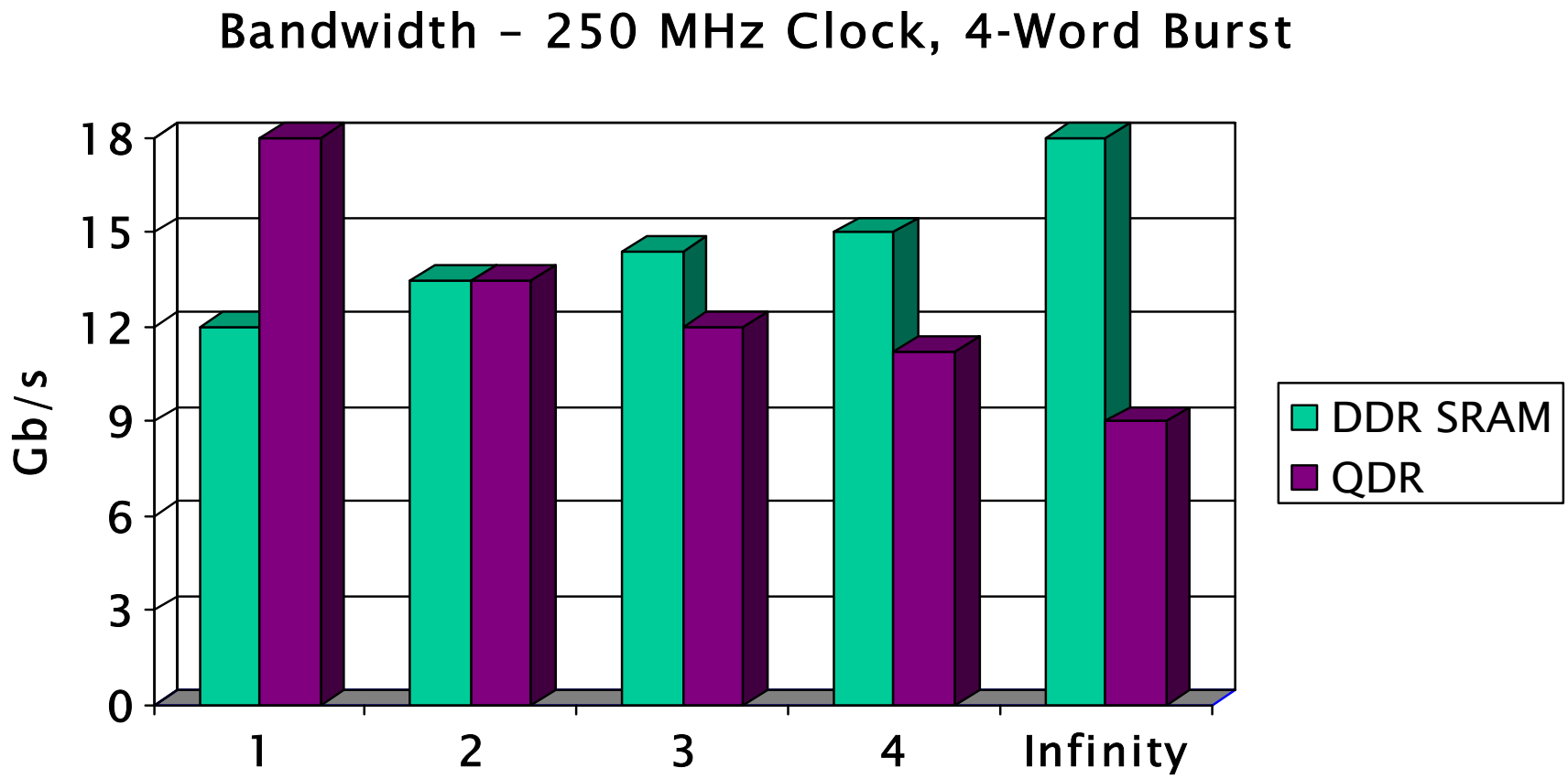
Bandwidth vs. Read/Write Ratio



Note: Assumes single x18 (per port) QDR device versus x36 DDR, burst of 4.
R/W refers to repetitive ratio between READ and WRITE cycles.

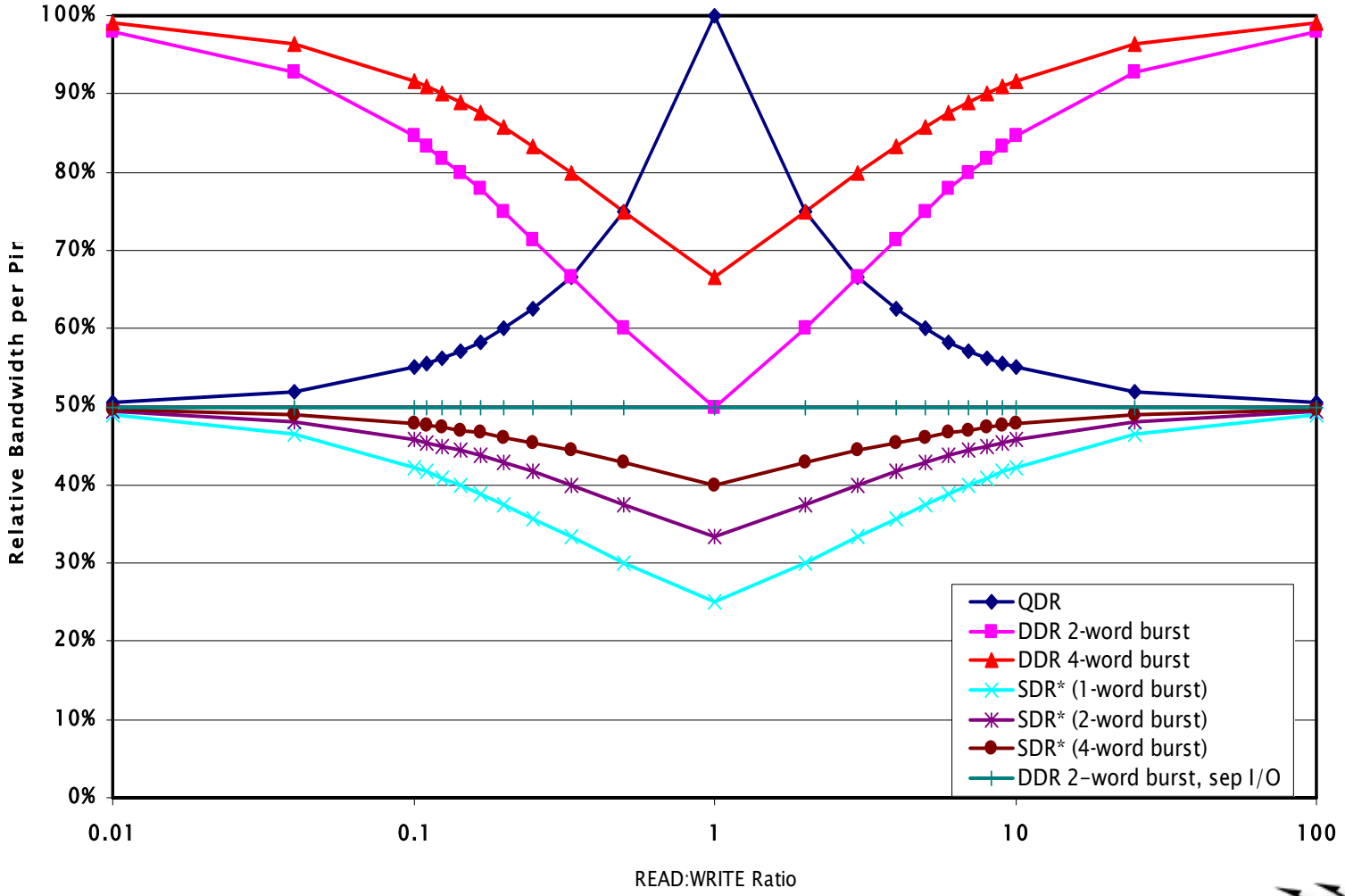
DDR maximum clock frequency is higher than QDR.

Bandwidth vs. Read/Write Ratio



Note: Assumes single x18 (per port) QDR device versus x36 DDR, burst of 4.
R/W refers to repetitive ratio between READ and WRITE cycles.

Relative Bandwidth per Pin of All Network SRAMs at 250 MHz Clock



*Note: SDR represents bandwidth per pin for NoBL, ZeroSB, NtRAM, and ZBT devices

Optimal Choices

Device	QDR	DDR SRAM
2-word burst	R/W < 3:1 2 Addr/Clock	R/W > 3:1 1 Addr/Clock
4-word burst	R/W < 2:1 1 Addr/Clock	R/W > 2 1 Addr/2 Clock

Note: R/W means ratio of READ cycles to WRITE cycles, or WRITE cycles to READ cycles

Clocks

- **Source clocks K, K# required**
  - Signals to SRAM synchronized to K, K#
- **Data clocks C, C# optional**
  - Output data from SRAM synchronized to C, C# if present; synchronized to K, K# if C, C# not present
- **Echo clocks CQ, CQ# optional**
  - Output clocks from the SRAM
  - Data is closely matched to CQ, CQ#
    - Latest technology permits 0.1ns matching
  - Acts as a “data valid” indication

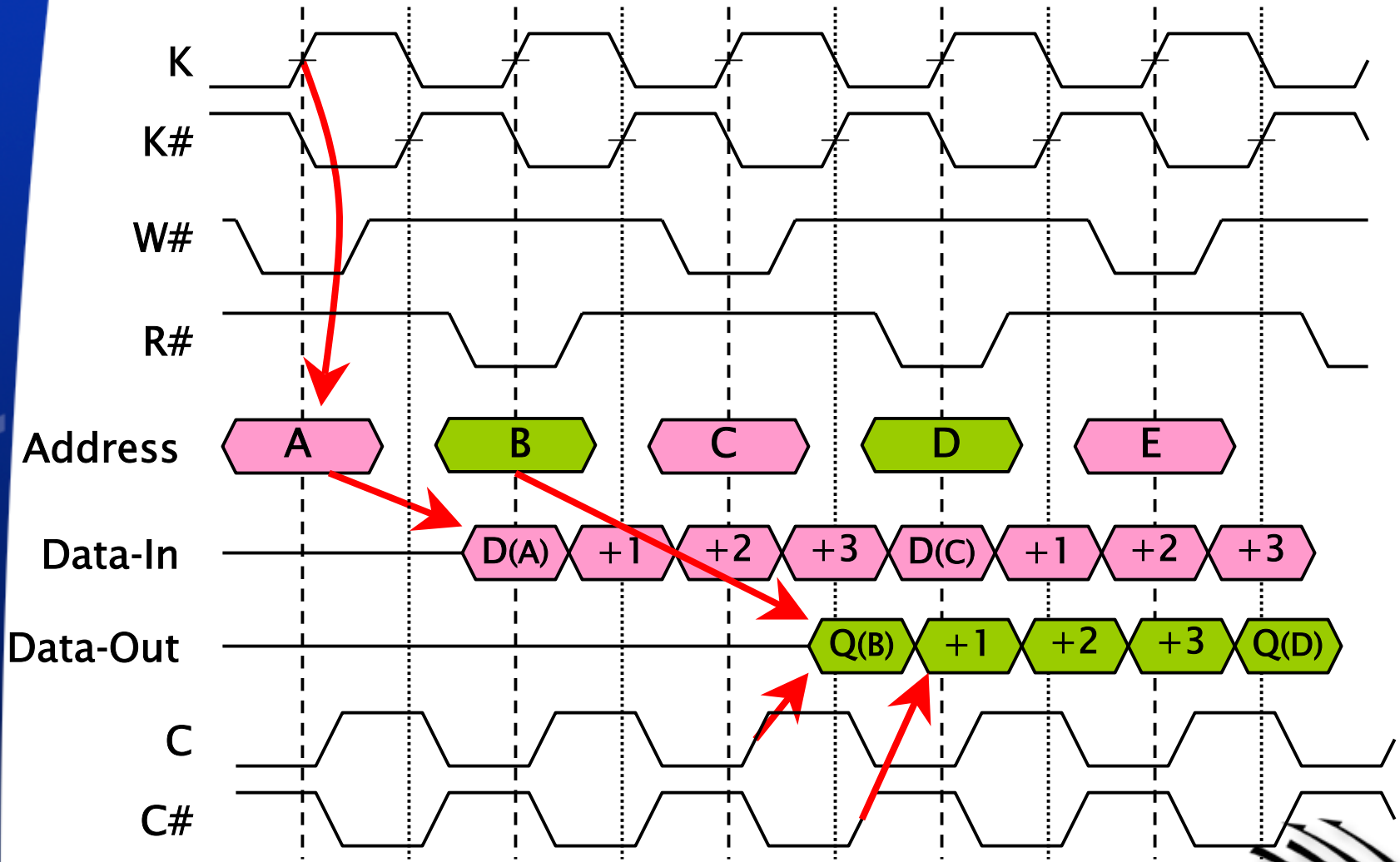
Packaging

- 13mm x 15mm, 1mm pitch, 11 x 15 grid FBGA
- 40% smaller than 14mm x 22mm BGA
- 55% smaller than 100-pin TQFP
- Signals all route on outer pins
- Easy clamshell design
  - Offers width or depth expansion
- Best high-frequency characteristics
- Shortest physical system bus – lower propagation delay

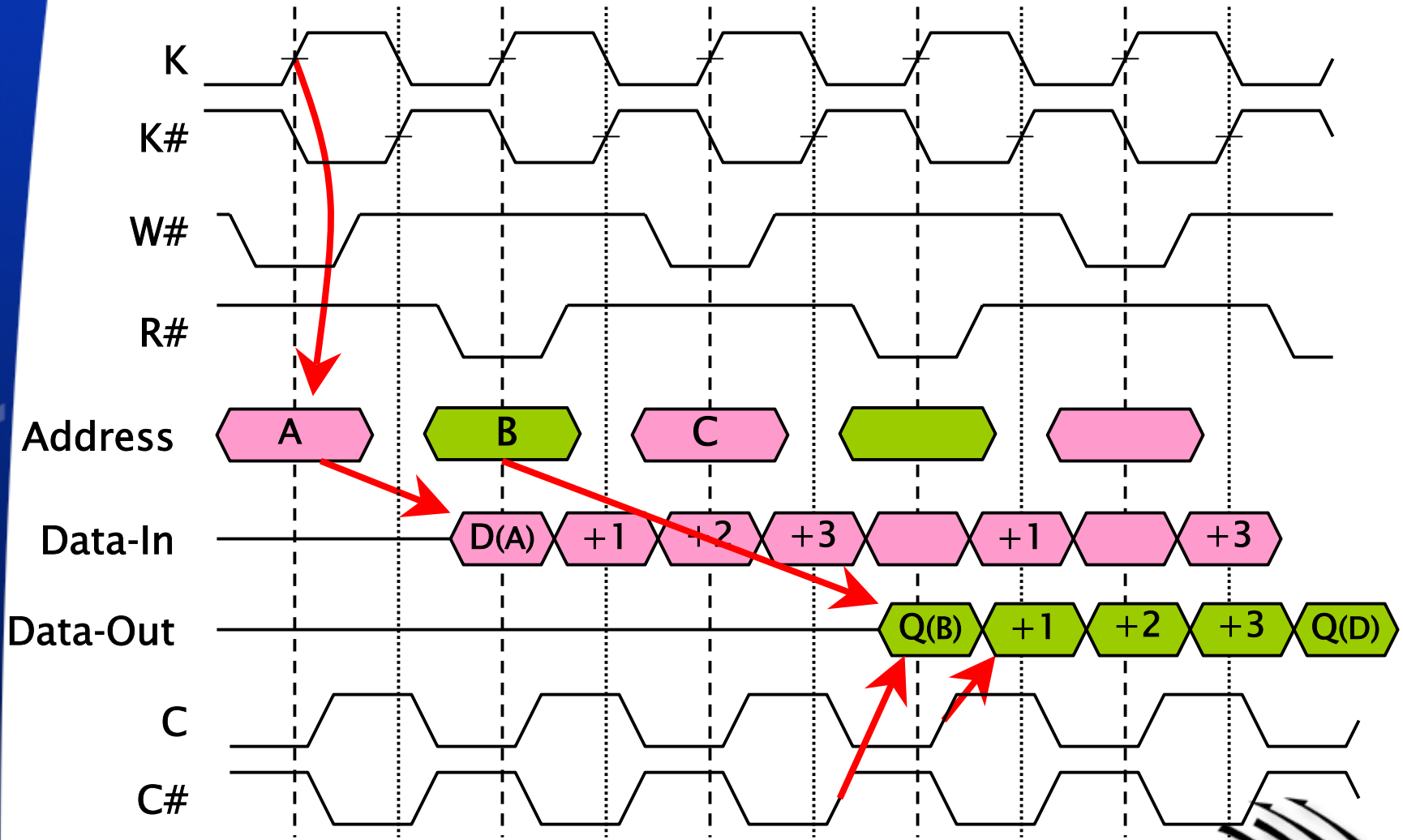
Mechanical Comparison

	TQFP	SIGMA BGA	FBGA
Pins/balls	100	11 x 19	11 x 15
Pin pitch (mm)	0.65	1.0	1.0
Package width	16.0	14.0	13.0
Package length	22.1	22	15
Package height	1.60	2.20	1.20
Minimum board area (mm^2)	353.6	308	195
Relative board area with via relief	1.0	0.71	0.45
Manufacturing cost	1.0	2.5	1.0
Footprint compatibility (compared with other SRAMs)	1Mb–18Mb	1Mb–144Mb	1Mb–288Mb

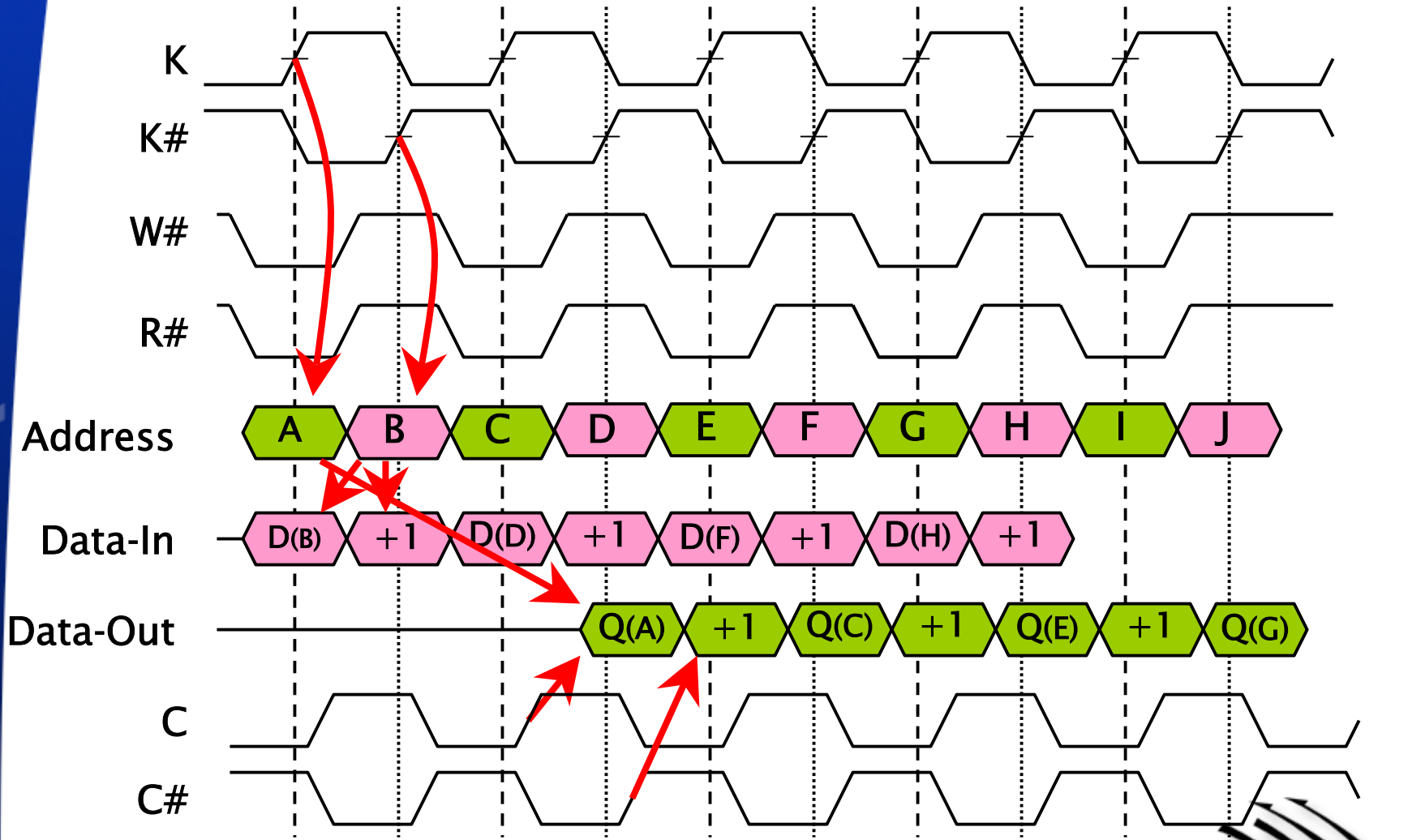
QDRI R/W Timing Diagram
(4-Word Burst)



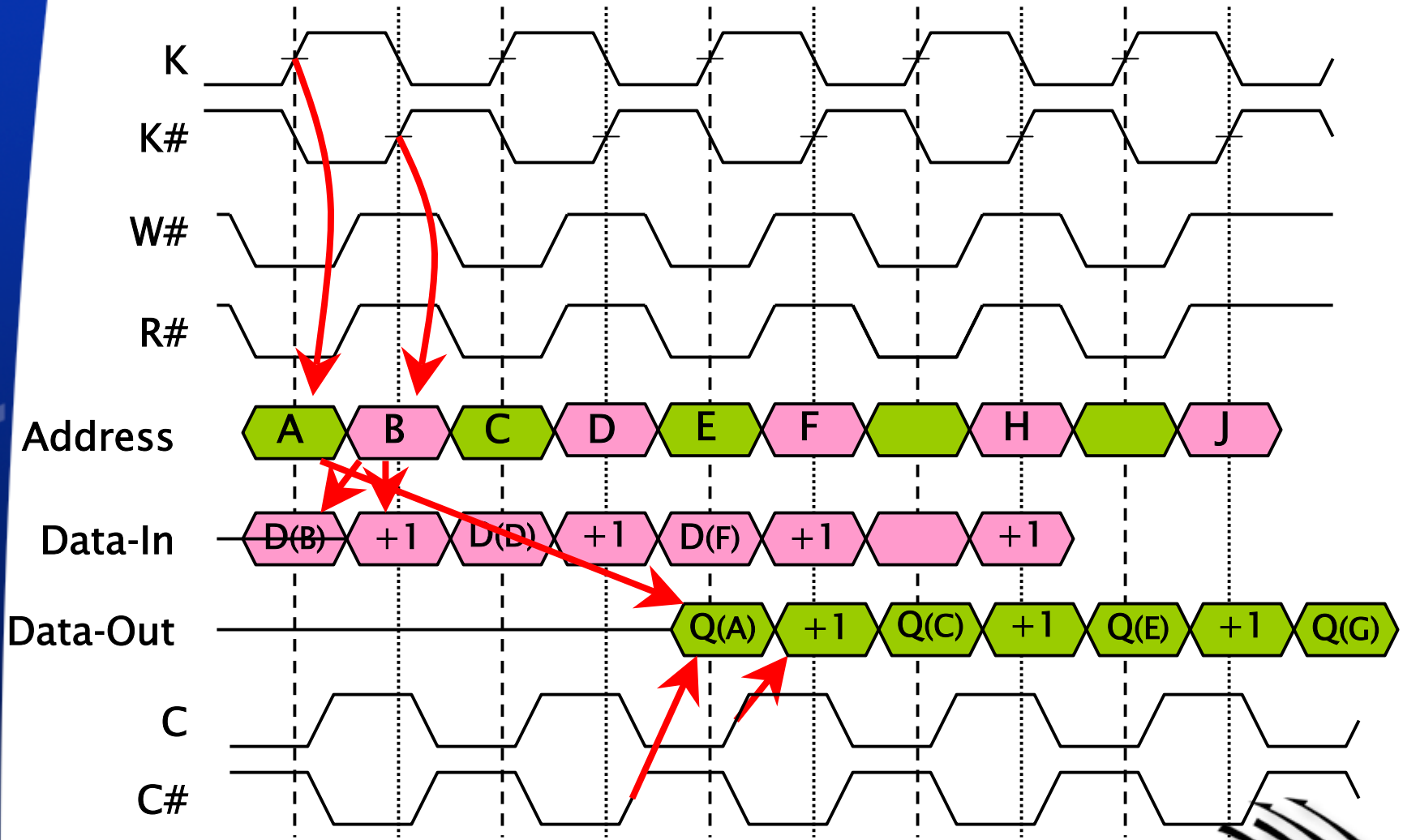
QDRII R/W Timing Diagram
(4-Word Burst)



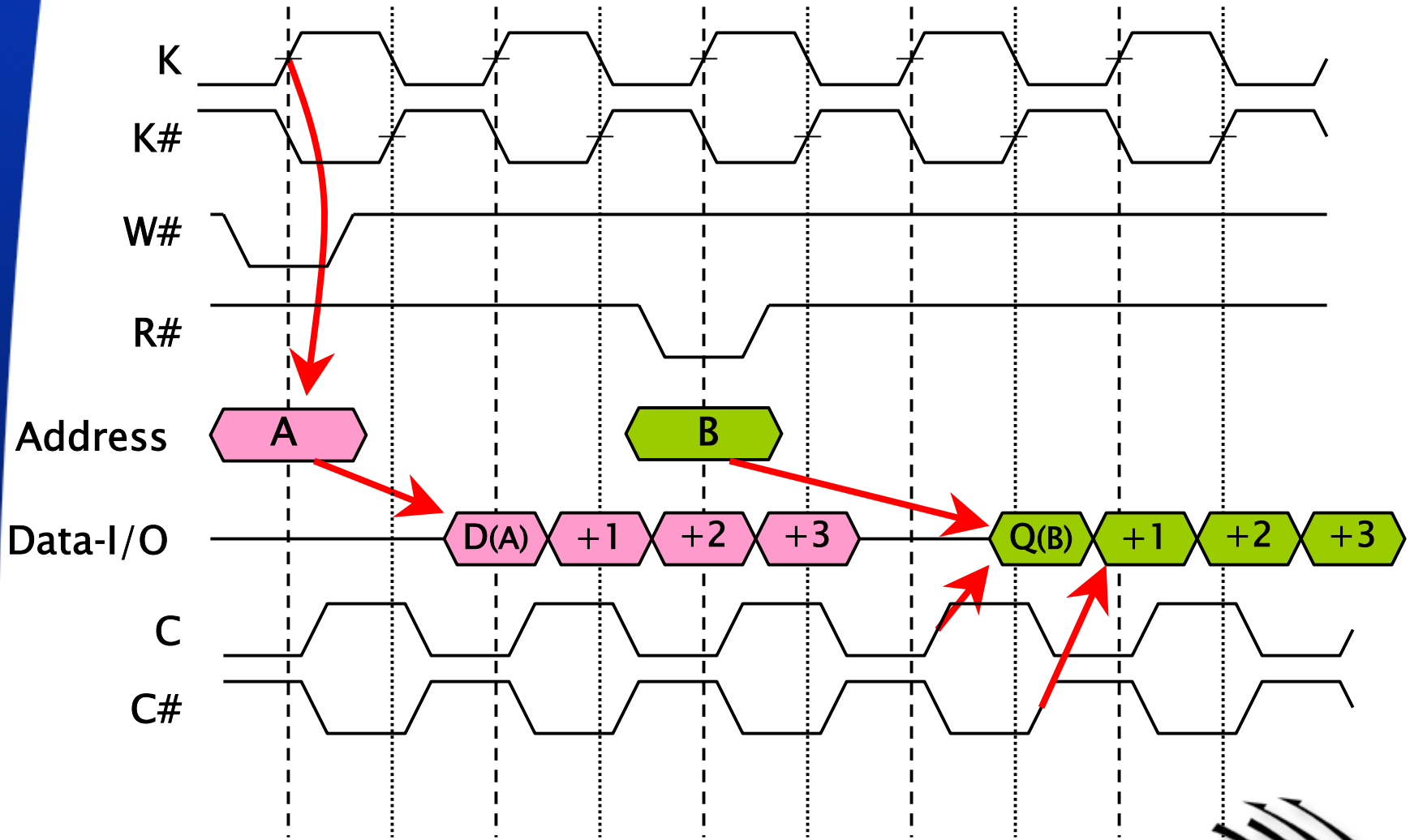
QDRI R/W Timing Diagram
(2-Word Burst)



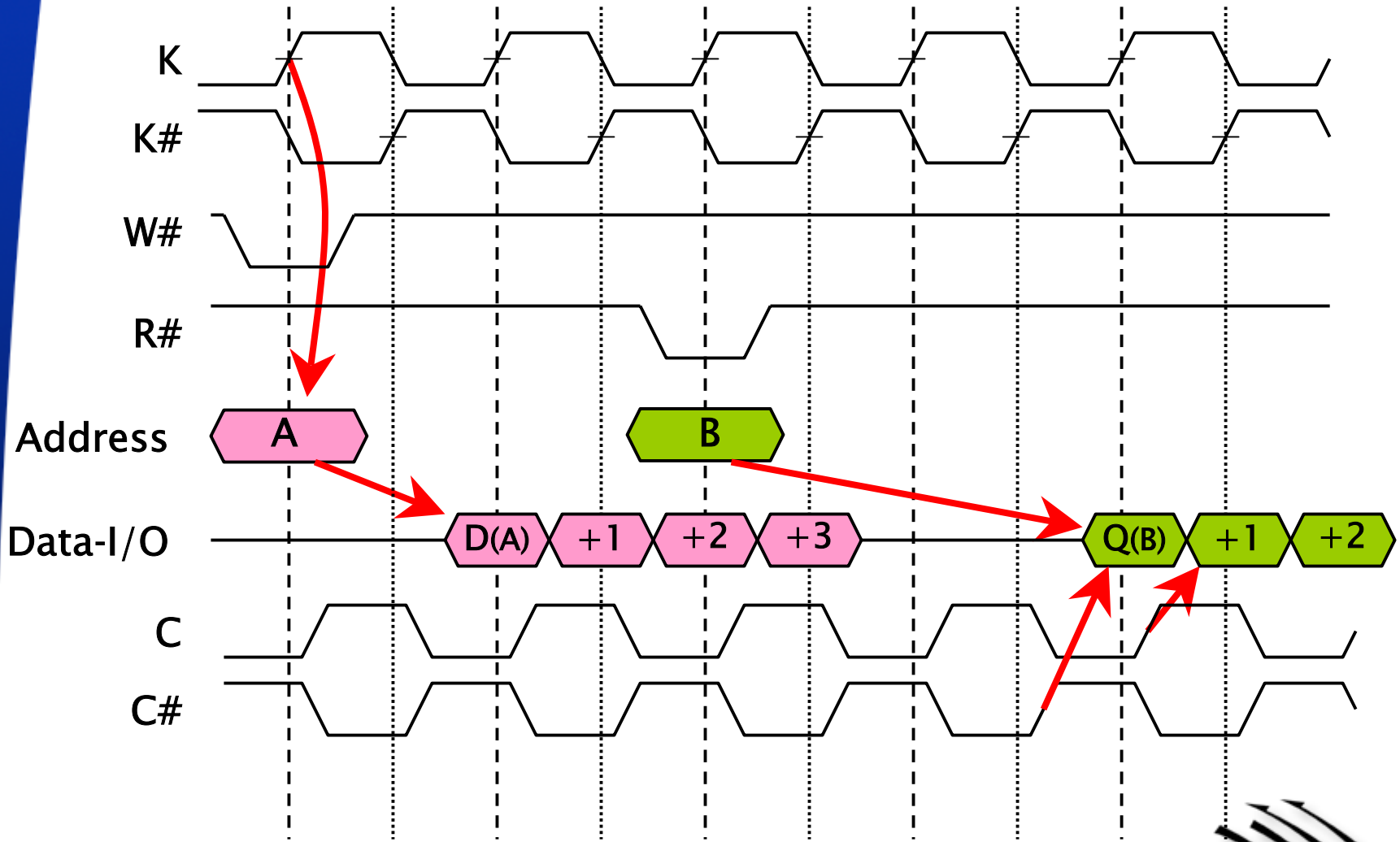
QDRII R/W Timing Diagram
(2-Word Burst)



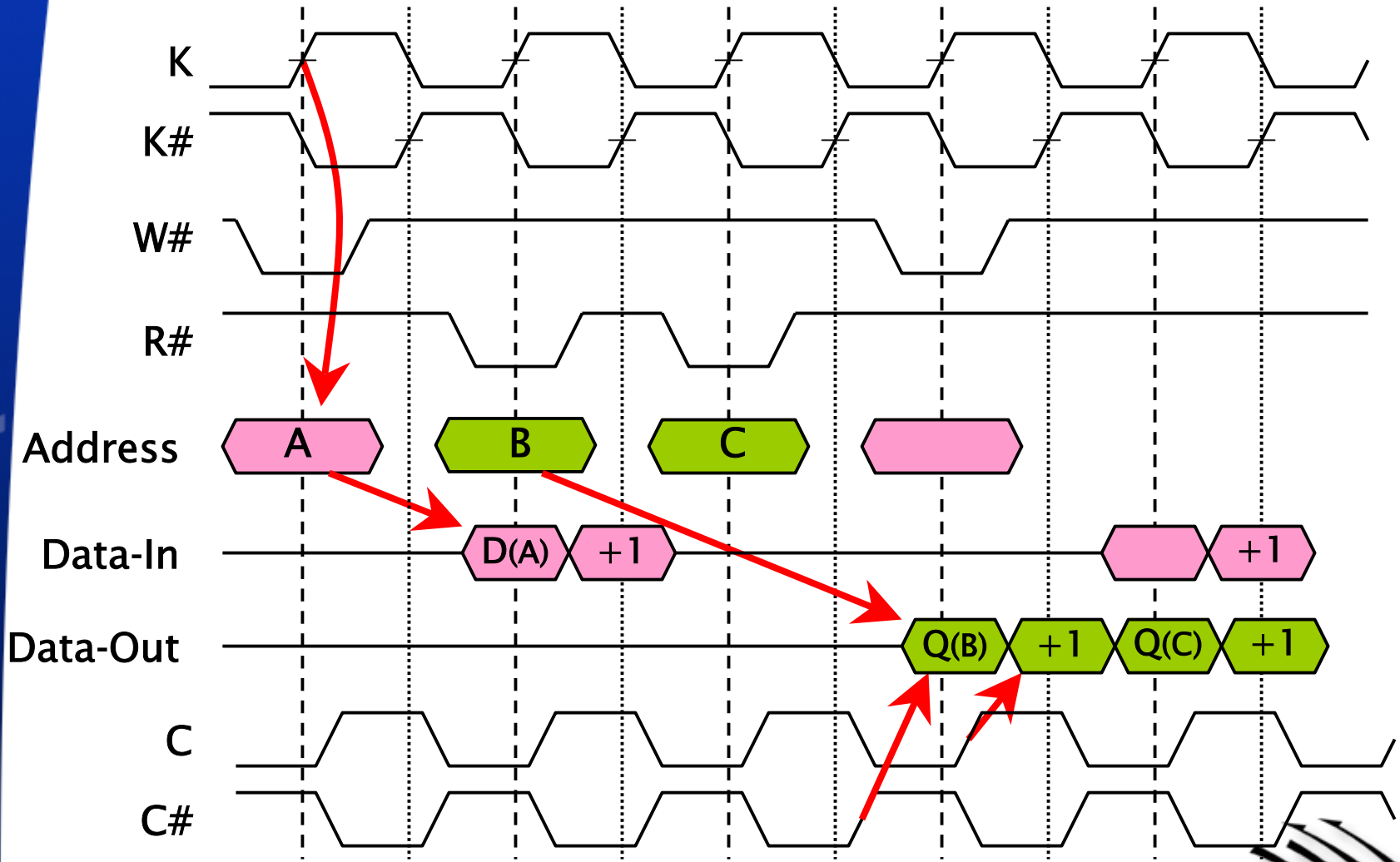
DDRI CIO R/W Timing Diagram
(4-Word Burst)



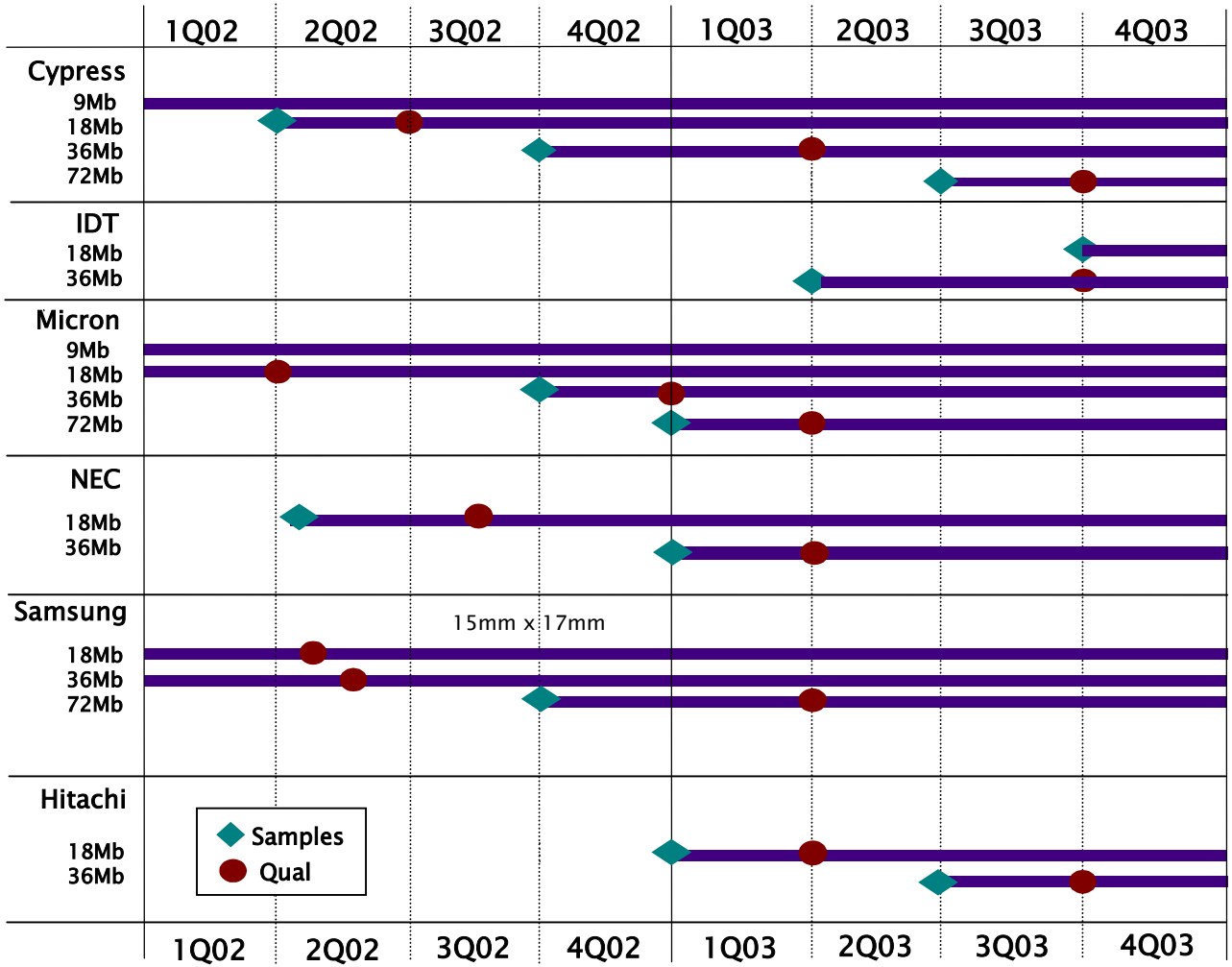
DDRII CIO R/W Timing Diagram
(4-Word Burst)



DDRII SIO R/W Timing Diagram
(2-Word Burst)



QDR/DDR SRAM Road Map



QDR RAMs and Quad Data Rate Rams comprise a family of products developed by Cypress Semiconductor, IDT, Micron Technology, Inc., NEC, and Samsung. Dates are estimates only. All information is subject to change. Rev. 4/02

Summary

- QDR is optimized for systems with short-term-balanced READ and WRITE operations
  - Packet memory
  - FIFO-like applications
- DDR is optimized for data streaming operations or READ/WRITE unbalanced systems
  - Chunks of READs or WRITEs
  - Look-up tables
  - Microprocessor, network processor, DSP memory
- DDR Separate I/O is optimized for one address/clock, 2-word burst systems
  - Minimized bus latency, maximized frequency
- Together, QDR and DDR enable any system design