

# QDR™-III: Next Generation SRAM for Networking

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# Agenda

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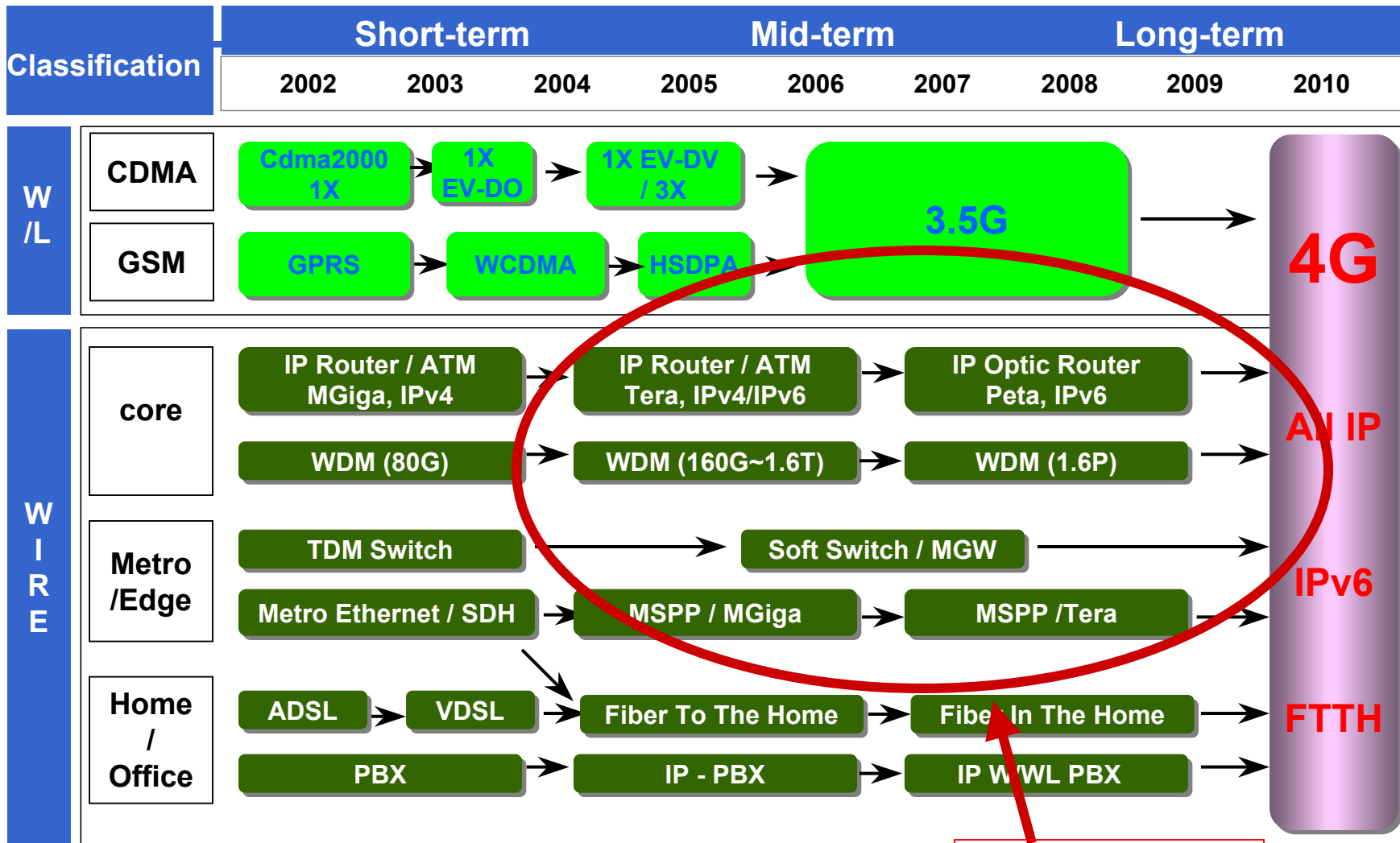
- ❑ QDR SRAMs – What are they good for?
- ❑ Existing QDR & QDR-II summary table
- ❑ QDR-III Features
- ❑ Samsung QDR SRAM Roadmap
- ❑ Summary

# QDR SRAM – What's it Good For?

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- ❑ QDR SRAMs are defined by the QDR Consortium
  - Cypress, IDT, Renesas, NEC, and Samsung
  
- ❑ QDR stands for Quad Data Rate™ – a family of SRAMs with separate Inputs and Outputs that each operate at Double Data Rates
  - QDR SRAMs, because of their concurrent read/write ability, are best used in applications where the read-to-write ratio is close to 1.

# Network Systems Evolution



\* FTTH : Fiber To The Home,  
NGN : Next Generation Network,

MSPP : Multi service provision platform  
WDM : Wavelength division multiplexing

QDR Target  
Usage

# Requirements for Network SRAMs

## □ Depth needed Lookup

~ 2003

2003 ~ 2005

2006 ~

**Forwarding Lookup**

**Classification**

**IPv6**

- ✓ **Lookup Entry**
  - Hundreds of Thousands
- ✓ **Memory Depth**
  - ~4Mbyte

**18M/36MBit**

- ✓ **Lookup Entry**
  - Several Millions
- ✓ **Memory Depth**
  - Several Tens Mbyte

**36M/72MBit**

- ✓ **Lookup Entry**
  - Several Tens Millions
- ✓ **Memory Depth**
  - Several Hundreds Mbyte

**72M/144MBit**

# QDR and QDR-II

Design Issue	QDR	QDR-II
Frequency Maximum	B2: 167MHz B4: 200 MHz	B2: 250 MHz B4: 333 MHz
Frequency Minimum	None	120 MHz
DLL	No	Yes
Initial Latency	1 clock cycles*	1.5 clock cycles*
Clocks	No echo clocks	Echo clocks
Density	9Mb / 18Mb / 36Mb	18Mb / 36Mb / 72Mb+
Power Supply	2.5V	1.8V



# QDR-III

# QDR-III Still Being Defined.....

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- ❑ As of May 2004, the QDR-III specification is still being defined by the QDR Consortium.
- ❑ The Consortium consists of Cypress, IDT, NEC, Renesas, Samsung.
- ❑ This presentation will outline the features of QDR-III.

# QDR-III Scope

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## □ QDR-III target product line-up

### ➤ QDR-III b2

- 2-word burst, separate IO concurrent read and write
- Frequency range: 250-500 MHz

### ➤ QDR-III b4

- 4-word burst, separate IO concurrent read and write
- Frequency range: 250-500 MHz

### ➤ DDR-III b2

- 2-word burst, common IO
- Frequency range: 250-500 MHz

# QDR-III Direction

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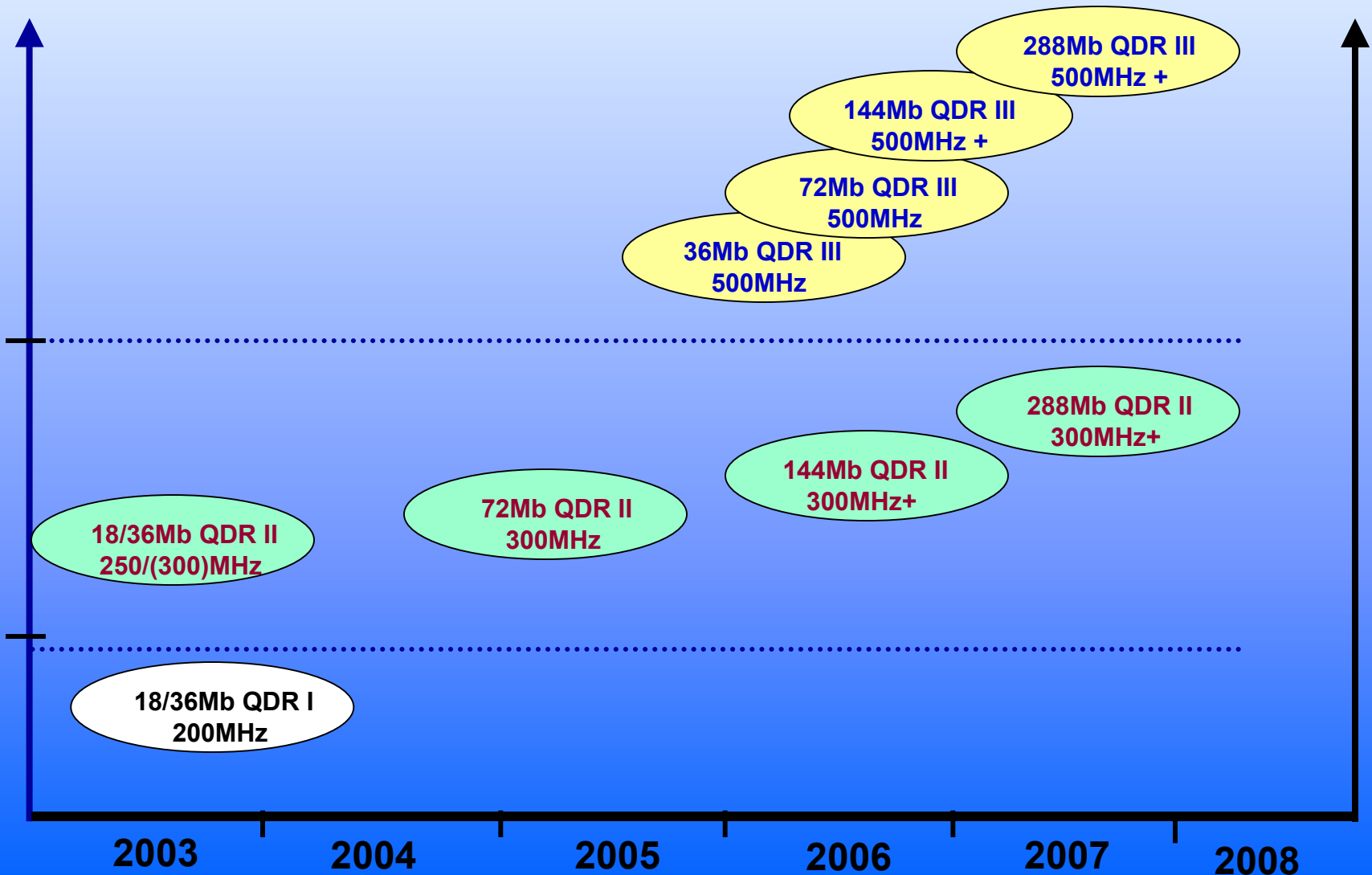
- ❑ All Consortium Members plan to support the versions listed on the previous pages with their designs
  - Currently, our customer surveys indicate that 4 versions will be the most popular...
    - ❑ QDR-III x18 burst of 4
    - ❑ QDR-III x18 burst of 2
    - ❑ QDR-III x36 burst of 4
    - ❑ DDR-III Common IO x36, burst of 2
- ❑ We recommend that customers consider these versions first
  - If they will not meet your needs, please contact us

# QDR-III Features

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- ❑ Voltage – 1.2V Vdd+/-5%
  - 1.2V Vddq +/-5% all speeds 250 – 500 MHz
- ❑ QDR-III Density range 18 Mb – 288 Mb
  - X9, x18, x36 widths
- ❑ Industry Defined Interface Standards
  - 1.2V JESD8-16 Compliant (BIC)
  - Network Processing Forum LA-1B Compatible ([www.npforum.org](http://www.npforum.org))
- ❑ Read latency, input/output impedance and termination, clocking schemes, pinout, etc
  - all available under NDA

# Samsung QDR SRAM Roadmap



# QDR-III Summary

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- ❑ The QDR Consortium, consisting of Industry Leaders in SRAMs, is working to craft a network-oriented SRAM for solid performance at a reasonable price for the 250MHz-500MHz range.
- ❑ The QDR Consortium is also planning for performance that exceeds 500MHz. Let us know your thoughts for those performance targets.

# QDR-III Conclusion

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- ❑ For Network Customers who want to know more about QDR-III.....
  - Contact QDR Consortium Members for NDA and further details...
  - Visit [www.qdrsram.com](http://www.qdrsram.com) website
  
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Quad Data Rate™ and QDR™: QDR is a trademark of the QDR Consortium